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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,673	06/25/2003	Kazuhito Matsukawa	239120US0 DIV	1975
22850	7590	02/10/2006	EXAMINER	
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.			ERDEM, FAZLI	
1940 DUKE STREET			ART UNIT	
ALEXANDRIA, VA 22314			PAPER NUMBER	
			2826	

DATE MAILED: 02/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/602,673	Applicant(s) MATSUKAWA, KAZUHITO	
	Examiner Fazli Erdem	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 November 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-4,6,8-12 and 17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4,6,8-12 and 17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 2 and 4 rejected under 35 U.S.C. 102(e) as being anticipated by Tachimori et al. (5,918,151).

Regarding Claim 2, Tachimori et al. disclose a method of manufacturing a semiconductor substrate and an apparatus for manufacturing the same where in Figs. 1C and 2B, it is disclose a semiconductor substrate 1 having a first and second surfaces, an oxide film 3 apart from the first and second surfaces extending throughout the semiconductor substrate 1, where the distance between the oxide film and second surface corresponds to on the order of 10^{-3} of a thickness of semiconductor substrate since the thickness of layer 2 is on the order to 5 micrometers and the thickness of the substrate is 500 micrometers.

Regarding Claim 4, Tachimori uses buried oxide layer 90-230 nm. However, in column 3, it teaches the use of buried oxide layer of 400 nm

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

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having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 6 and 8, rejected under 35 U.S.C. 103(a) as being unpatentable over Tachimori et al. (5,918,151) in view of Aspar et al. (6,110,802).

Regarding Claims 6 and 8, Tachimori et al. disclose a method of manufacturing a semiconductor substrate and an apparatus for manufacturing the same where in Figs. 1C and 2B, it is disclose a semiconductor substrate 1 having a first and second surfaces, an oxide film 3 apart from the first and second surfaces extending throughout the semiconductor substrate 1, where the distance between the oxide film and second surface corresponds to on the order of 10^{-3} of a thickness of semiconductor substrate since the thickness of layer 2 is on the order to 5 micrometers and the thickness of the substrate is 500 micrometers. Tachimori et al discloses silicon layer on top of the oxide layer. Tachimori et al. fail to specify this layer to be epitaxial layer. However, Aspar et al. disclose a process for producing a structure with a low dislocation density comprising an oxide layer buried in a semiconductor layer where in Fig. 3, epitaxial layer 14 is located on buried oxide layer 6.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required epitaxial layer on oxide layer in Tachimori et al. as taught by Aspar et al. in order to have a semiconductor device with increased functionality and performance.

4. Claims 1, 3 and 9-12 rejected under 35 U.S.C. 103(a) as being unpatentable over Masanori et al. (5,834,363) in view of Sato (2002/0127820).

Regarding Claims 1, 3 and 9-12, Masanori discloses a method of manufacturing semiconductor wafer, semiconductor wafer manufacturing by the same semiconductor epitaxial wafer and method of manufacturing where in Fig. 3D, it is disclose a substrate 4 having a first and second surfaces, an oxide film 5, extending throughout the semiconductor substrate, where the oxide film 5 is closer to the second/lower surface where the epitaxial layer 7 is disposed on the first/upper surface. Masanori fails to disclose that the oxide layer apart from the second surface. However, Sato discloses a semiconductor substrate and method for producing the same where in Fig. 10e, oxide layer 14 is disclosed to be apart from the second surface of the semiconductor substrate.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required oxide layer apart from the lower/second surface of the substrate in Masanori as taught by Sato in order to have semiconductor device with increased reliability and auto-doping control.

Regarding Claims 3, 11 and 12, Masanori discloses oxide film layer thickness of 500 nm in column 6, example 1.

Regarding Claim 10, layer 12 in Sato is in the order of 5 micrometers and the substrate thickness is 500 micrometers

5. Claim 17 rejected under 35 U.S.C. 103(a) as being unpatentable over Masanori et al. (5,834,363) in view of Sato (2002/0127820) further in view of Mitani et al. (5,306,939)

Regarding Claim 17 Masanori discloses a method of manufacturing semiconductor wafer, semiconductor wafer manufacturing by the same semiconductor

epitaxial wafer and method of manufacturing where in Fig. 3D, it is disclose a substrate 4 having a first and second surfaces, an oxide film 5, extending throughout the semiconductor substrate, where the oxide film 5 is closer to the second/lower surface where the epitaxial layer 7 is disposed on the first/upper surface. Masanori fails to disclose that the oxide layer apart from the second surface and the required substrate with the boron concentration. However, Sato discloses a semiconductor substrate and method for producing the same where in Fig. 10e, oxide layer 14 is disclosed to be apart from the second surface of the semiconductor substrate. Furthermore, Mitani et al. disclose epitaxial silicon wafers for CMOS integrated circuits where substrate 20 has boron concentration of $3 \times 10^{18} \text{ cm}^{-3}$.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required oxide layer apart from the lower/second surface of the substrate and the required boron concentration in the substrate in Masanori as taught by Sato and Mitani et al. in order to have semiconductor device with increased reliability and auto-doping control.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fazli Erdem whose telephone number is (571) 272-1914. The examiner can normally be reached on M - F 8:00 - 5:00.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

FE

January 27, 2006



NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
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